

Electrical Tests of SCT Hybrids and Modules

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Abstract

This document aims to describe each of the electrical (readout) tests of SCT hybrids and modules that will be performed during production. A number of test sequences designed to simplify the task at hand are also presented.

The methodology of each test and the subsequent analysis of its data are outlined. A number of possible defect types that can be identified by each test is given, and a table of values to be recorded in the ATLAS SCT production database is defined. In each case an example is included of the ASCII file output by the analysis software and designed to be read into the production database.

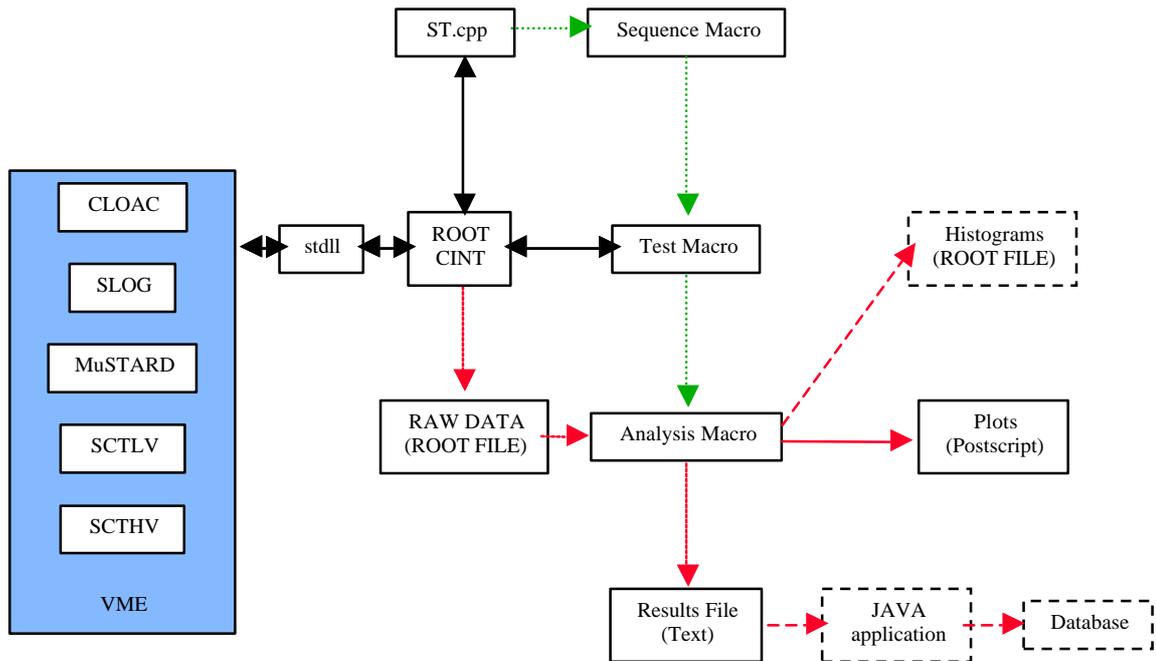
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System Overview

Introduction

This section outlines the mechanism used to run each test, right through to the point at which the data has been recorded in the database. Use of MuSTARD, SLOG and SCTLV hardware has been assumed, together with the SCTDAQ¹ software package. Ideally a CLOAC module would be used, particularly for studies of noise occupancy, but in all cases a sensible backup option has been provided using only SLOG. SCTHV may also be used to provide detector bias to the modules under test.



The basic routines to communicate with each VME board are implemented in the form of a static library written in C. Higher level functions have been implemented in a small number of C++ classes that are linked together with the static libraries, and some of the ROOT libraries, to form the dynamic link library `stdll`. This is the full extent of the compiled code: everything else runs through the CINT interpreter.

Within ROOT, the user runs the top-level macro `ST.cpp` to load `stdll`, to initialise the system and to present the system menu. Each of the proposed electrical tests has been implemented in the form of a discrete ROOT macro which may be run by pressing a button within the menu system, by running an overall “sequence macro” or by direct user input at the command prompt. At the end of each scan a ROOT file is generated which contains the scan data for each module, records of error and event counters and some module configuration and DCS information.

Analysis of the raw data from each test is performed by a separate root macro which appends results to a text file, one per hybrid or module per day, such that the results of each test in the sequence are kept together in one file. It is foreseen that one or more Java applications will be written to upload this data and any associated raw data files directly into the database¹. For most tests, results may also be output in the form of plots within a postscript file. In future the software may be revised to keep a number of the derived histograms for each module together in a separate root file.

¹ In order to upload the results to the database, one file for each *test* is needed rather than one file for each *test sequence*. A simple script will be written to split the results file into a number of segments appropriate to the upload procedure. The files will be deleted after upload.

Test results and the SCT Database

The following table is reproduced from the list of [SCT Database table definitions](#).

TESTS: General Details of Tests on Items

Column Name	Type	Description
SER_NO	Long int	Atlas serial no. of item
TEST_NO	Long int	ID no. of test
RUN_NO	Char(80)	Data taking run no.
TEST_NAME	Char(20)	Name of test
TEST_DATE	Date	Date of test
LOCN_NAME	Char(50)	Location of test
INITLS	Char(4)	Initials of user
PASS	Boolean	Passed unconditionally?
PROBLEM	Boolean	Problems encountered?
SUBSYST	Char(1)	Subsystem code
LAST_MOD	Date	Date record last updated
OWNER	Char(30)	Owner institute of the record
Primary Key:	TEST_NO	
Foreign Key:	SER_NO	ITEMS(SER_NO)
Foreign Key:	TEST_NAME	TEST_DESCR(TEST_NAME)
Foreign Key:	LOCN_NAME	LOCNS(LOCN_NAME)
Foreign Key:	INITLS	PERSONS(INITLS)

For each electrical test performed upon a hybrid or module an instance of the above object will be added to the database, hence the serial number, run number, location and tester are always recorded. Digital tests will set the "PASS" field to "NO" if more than a specified number of defects are found, but in general the analogue tests do not make use of this field. The "PROBLEM" field is not used by the electrical test software and is set to "NO" in all cases. The remaining fields shown in the above table are for internal use by the database.

Information specific to each electrical test is recorded in one or more data tables, defect objects and/or raw data files, all of which are linked to the relevant instance of the basic test object described above.

A number of utility tables have been designed to store information that it is desired to record for a number of tests, such as monitored DCS parameters. This has greatly simplified the definition of the tables needed to store the results of each specific test, since all common factors have been removed. The definitions of the utility tables can be found in [appendix 1](#).

In addition to the utility tables, a table has been designed to record the results of each test. These tables are defined in [appendix 2](#). There is a direct link to each table from the relevant section of the text.

The list of defects that may be identified by each test are detailed in the test and summarised in [appendix 3](#).

Additional configuration information or more detailed results may be stored in the form of (ASCII) raw data.

A list of all database tables specific to the electrical testing of hybrids and modules, showing their implementation status, can be found in [appendix 4](#).

The Format of the Results File

Results from each test are appended to a file:

```
sctvar\results\serialnumber_YYYYMMDD.txt
```

For example:

```
sctvar\results\20220170100016_20010821.txt
```

The following tag is used to indicate the start of a new section, corresponding to a new test:

```
#  
%NEW_TEST
```

This is followed by a section containing information stored in the basic test entity:

```
#  
SERIAL NUMBER : 20220170100016  
TEST MADE BY  : pwp  
LOCATION NAME   : RAL  
Run number    : 256-11  
TEST_DATE     : 09/08/2001  
PASSED        : YES  
PROBLEM       : NO
```

Next comes a section describing the IP name of the host computer, the software version number and the time of the test, corresponding to the utility table [TSTDAQINFO](#):

```
#  
%DAQ_INFO  
#  
#HOST  
"HEPNTW124"  
#VERSION  
"3.10"  
#DUT  
"Barrel Module"  
#TIME  
"18:15:18"
```

The next section gives the monitored DCS values, corresponding to the utility table [TSTDCSINFO](#):

```
#  
%DCS_INFO  
#  
#T0      T1  
25.5    26.3  
#VDET    IDET  
350     1.220  
#VCC     Icc  
3.500   790  
#VDD     IDD  
4.000   535
```

Depending upon the test which has been executed, there may now follow a section giving details of the number of scans used to make a measurement and the corresponding fixed parameter used for each of those scans. This information is stored in the utility table [TSTSCANINFO](#). The following example lists the number of scans and charges used to make a three point gain measurement:

```
#
%SCAN_INFO
#
#POINT TYPE
"QCAL (fC)"
#N_POINTS
3
#POINTS
1.50 2.00 2.50
```

The actual results of the test are summarised in the following section, corresponding to the table specific to that test. By way of an example, here is the format used to list the results of the [StrobeDelay](#) test:

```
#
%StrobeDelay
#
#DELAY
#M0 S1 S2 S3 S4 E5
-1 -1 -1 -1 16 17
#
#M8 S9 S10 S11 S12 E13
17 15 16 16 16 18
#
```

A list of defects is generated if any defects were found by the test. The types of defect that are identified by each test are described in the corresponding section of this document and summarised in [appendix 3](#). Each defect is prefaced by the tag "%Defect".

Here is a list of defects found by the [StrobeDelay](#) test:

```
%Defect
DEFECT NAME : SD_LO
FIRST CHANNEL : 0
LAST CHANNEL : 127
#
%Defect
DEFECT NAME : SD_LO
FIRST CHANNEL : 128
LAST CHANNEL : 255
#
%Defect
DEFECT NAME : SD_LO
FIRST CHANNEL : 256
LAST CHANNEL : 383
#
%Defect
DEFECT NAME : SD_LO
FIRST CHANNEL : 384
LAST CHANNEL : 511
#
#4 defects found
#
```

Finally, any raw data files which are to be associated with the test are listed.

```
%TEST Rawdata
FILENAME : D:\sctvar\results\20220170100016_rc_246-12.txt
```

Further examples are given throughout the remainder of the document.

Sequences and Optional Extras

Before Running a Sequence

The following tests do not apply to all devices, hence they have been omitted from the characterisation and confirmation sequences. It is left to the user to run them manually as required by means of the menu system.

DC Test:

- [IVCurve.cpp](#) (modules only)

Digital Tests:

- StreamDelay.cpp (implemented but not yet documented)
- Opto Functionality Tests (**forward only**) (not yet implemented)

CharacterisationTest.cpp

The Characterisation Sequence aims to verify the basic digital functionality of a hybrid or module, and to fully characterise its analogue performance. The menu system contains a button to start the sequence, which comprises the following tests:

Digital Tests:

- [HardReset.cpp](#)
- [RedundancyTest.cpp](#)
- [FullBypassTest.cpp](#)
- [PipelineTest.cpp](#)

Analogue Tests:

- [StrobeDelay.cpp](#)
- [ThreePointGain.cpp](#) (untrimmed)
- [TrimRange.cpp](#)
- [ResponseCurve.cpp](#)
- [NO.cpp](#)
- [Timewalk.cpp](#)

ConfirmationTest.cpp

The **Confirmation Sequence** aims to verify, as quickly as possible, that the performance of a hybrid or module has not deteriorated, perhaps as a result of handling or shipping.

The digital tests that are part of this sequence are chosen to help identify damaged wirebonds and the analogue tests, whilst sufficient to demonstrate that the basic performance is as expected, avoid the more time consuming tasks such as trimming or a measurement of the noise occupancy. The menu system contains a button to start the sequence, which comprises the following tests:

Digital Tests:

- [HardReset.cpp](#)
- [RedundancyTest.cpp](#)
- [FullBypassTest.cpp](#)

Analogue Tests:

- [StrobeDelay.cpp](#)
- [ThreePointGain.cpp](#) (trimmed or untrimmed, as appropriate)

Other Electrical Tests

Some of the tests listed in this section are mandatory, such as the long term test of the hybrid, and some are optional, such as a laser scan of the finished module. Not all of these tests have yet been written: in any case they are shown here as placeholders.

- [HybridLTT.cpp](#) (provisional version available)
- Laser Efficiency Scan (not yet implemented)
- Source Efficiency Scan (not yet implemented)

Description of DC Tests

IVCurve.cpp

This test has been designed for users of the SCTHV high voltage power supply module. Those without access to this module may wish to perform a similar test using other hardware. If the results are stored in the same format, they may still be uploaded to the database.

Method

An IV curve is taken raising the detector bias voltage from 10V to an upper limit of 150V, 350V or 500V as selected by the operator, always in 10V steps. (It is recommended that the number of times for which the module bias is taken to 500V should be kept as low as is possible).

A firmware current limit of 100 μ A, set high to allow for charging currents, is imposed throughout the sequence. If this limit is exceeded, the voltage will trip off. The current drawn at each voltage point is recorded 10 seconds after the requested voltage has been reached. In addition, should a module draw more than 10 μ A current after the 10 second wait time, the voltage applied to that module will not be raised further. Upon completion of the test, the bias voltage is turned down to 150V, the standard used during analogue tests of unirradiated modules.ⁱⁱ

During production testing this test would usually be performed before the chip bias has been applied but there may be exceptions to this rule, hence it is necessary to record the voltages supplied to, and the currents drawn by, the hybrid. This is achieved by sampling all monitored DCS parameters when the bias voltage has reached its highest point. The information is recorded within an instance of the database table TSTDCSINFO.

Analysis

If a current drawn by a module exceeds the lower limit of 10 μ A, the defect IV_LIMIT is recorded. If the high voltage supply connected to a module trips off, the defect IV_TRIP is recorded.

Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures
TSTMODIV: leakage currents at 150V and 350V

DEFECTS:

Defect	First Channel	Last Channel
IV_LIMIT	0	1535
IV_TRIP	0	1535

RAW DATA:

ABCD_CONFIG (optional)
IV_DATA (mandatory)

Acceptance

The database reporting structure should also provide the possibility to set stricter acceptance cuts on the range of acceptable detector bias current values, and to compare values against the sum of the currents drawn by the four detectors before assembly into a module.

ⁱⁱ The detector bias voltage used during tests of irradiated modules, subject to consideration of the detector leakage current, is typically 300V.

Sample Output from the Results File

```
#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY  : pwp
LOCATION NAME   : RAL
Run number    : 256
TEST_DATE     : 09/08/2001
PASSED        : YES
PROBLEM       : NO
#
%DAQ_INFO
#
#HOST
"HEPNTWL24"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"16:20:02"
#
%DCS_INFO
#
#T0      T1
25.5    26.3
#VDET    IDET
350     1.220
#VCC     ICC
0.000   0
#VDD     IDD
0.000   0
#
%ModIVScan
#
TEMPERATURE : 25.5
I LEAK 150  : 0.994
I LEAK 350  : 1.220
#
#No defects found!
#
%TEST Rawdata
FILENAME     : D:\sctvar\results\20220170100016_iv_20010824.txt
```

Description of Digital Tests

HardReset.cpp

Method

- The power is cycled such that all chips return to the power on condition. With the aid of an oscilloscope and following the guidance given by the software, the user must verify that each Master chip outputs clock divided by 2. Once this has been completed the currents I_{cc} and I_{dd} are recorded (ICC_NOCONFIG, IDD_NOCONFIG).
- A series of configuration commands is issued to set the clock feedthrough bit high and to program all DACs to nominal values as shown in the table below. The user is prompted to confirm that output of clock/2 by each Master chip has stopped. The currents I_{cc} and I_{dd} drawn in this configuration are recorded within an instance of the TSTDCSINFO table.
- The HARD RESET signal is issued. The user is prompted to check that once more each master chip outputs clock/2.
- The clock is momentarily turned off, and the analogue and digital currents I_{cc} and I_{dd} are recorded (ICC_NOCLOCK, IDD_NOCLOCK).

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E	
		Edge Detect													ON
		Data Compression													01X
		Mode													Data Taking Mode
		Select													0
		Masked Channels													None
	DACs	Ipreamp													220 μ A
		Ishaper													30 μ A
		Threshold DAC													100mV
		Calibration DAC													10mV (1.0fC)
		Delay Register													-
		TrimRange													0
		TrimDAC													0

Analysis

If either datalink should fail to output the clock/2 signal upon power up, that will be recorded as the defect HR_NOCLK. If clock/2 output does not cease upon transmission of the configuration sequence, the defect HR_NOCON is recorded. Finally, if clock/2 does not return after the HARD RESET signal, that is recorded as the defect HR_NORST.

Database

The following information should be stored in the SCT database:

- TSTDAQINFO**: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures
TSTHYBRESET: digital and analogue currents when not configured or when clock interrupted

DEFECTS:

Defect	First Channel	Last Channel
HR_NOCLK	Link * 768	((Link+1) *768) -1
HR_NOCON	Link * 768	((Link+1) *768) -1
HR_NORST	Link * 768	((Link+1) *768) -1

RAW DATA:

ABCD_CONFIG (optional)

Acceptance

None of the defects found by this test are allowable on production modules, hence the “PASS” field will be set to “NO” if any defects are found.

The database reporting structure should also provide the possibility to set acceptance cuts on the range of allowable current values Icc and Idd in each of the three cases.

Sample Output from the Results File

```
#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY  : pwp
LOCATION NAME   : RAL
Run number    : 256
TEST_DATE     : 09/08/2001
PASSED        : YES
PROBLEM       : NO
#
%DAQ_INFO
#
#HOST
"HEPNTW124"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"16:28:26"
#
%DCS_INFO
#
#T0      T1
25.5     26.3
#VDET   IDET
350      1.220
#VCC    ICC
3.500    790
#VDD    IDD
4.000    535
#
%HardReset
#NOCONFIG      ICC      IDD
                715     525
#NOCLOCK      ICC      IDD
                795     260
#
#No defects found!
#
#No raw data!
```

RedundancyTest.cpp

The hybrid or module is configured as described below by use of each clock/command pair. Since this test also aims to check the integrity of command reception, one of a number of defined mask patterns is written to each chip prior to each L1A trigger. Consecutive events use different mask patterns.

Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E	
		Edge Detect													OFF
		Data Compression													X1X
		Mode													MASK + Data Taking Mode
		Select													(variable)
		Masked Channels													(variable) - SEE BELOW
	DACs	Ipreamp													220 μ A
		Ishaper													30 μ A
		Threshold DAC													500mV
		Calibration DAC													10mV (1.0fC)
		Delay Register													-
		TrimRange													0
		TrimDAC													0
	TRIGGER	Sequence													Full Configuration + Soft Reset + 129 BCO delay + L1A
		Frequency													-
LOOPS	1 – SELECT													0,1	
	2 – MASK													Mask #1, #2	
n Triggers													100		

The mask patterns to be used are as follows:

1. a sequence of 010101...01
2. a sequence of 101010...10

Soft Reset is issued a specified number of BCOs before each L1A to ensure that each event is shifted through the same cells of the pipeline. In this way any channel affected by a dead cell in the pipeline can only have zero occupancy, and any difference in the occupancy of a channel for each setting of SELECT must have been caused by addressing or command reception errors.

Analysis

Each channel is categorised according to occupancy as follows:

nhits ₀ (select = 0)	nhits ₁ (select = 1)	
50	50	Good channel
100	100	Stuck channel
0	0	Dead channel (not yet able to resolve if pipeline or mask defect)
50	0 or 100	ID4 addressing error when select = 1
0 or 100	50	ID4 addressing error when select = 0
50	0 < n < 100	Command reception is not reliable when select = 1
0 < n < 100	50	Command reception is not reliable when select = 0
other	other	Command reception is never reliable

During the second stage of the analysis the numbers of channels of each chip which fall into each of the above categories is tallied leading to the categorisation of each chip as shown below. All failures are recorded as defects.

```

IF ((nch_good>120) AND (remainder STUCK OR DEAD))
    PASS code 0
ELSE IF (nch_addressing_error_0>120)
    FAIL code 1 (defect CLK_ADDR0)
ELSE IF (nch_addressing_error_1>120)
    FAIL code 2 (defect CLK_ADDR1)
ELSE IF (nch_command_error_0>120)
    FAIL code 3 (defect CLK_COM0)
ELSE IF (nch_command_error_1>120)
    FAIL code 4 (defect CLK_COM1)
ELSE FAIL code 5 (defect CLK_ERROR)

```

Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures

DEFECTS:

Defect	First Channel	Last Channel
CLK_ADDR0	Chip * 128	((Chip+1) * 128) -1
CLK_ADDR1	Chip * 128	((Chip+1) * 128) -1
CLK_COM0	Chip * 128	((Chip+1) * 128) -1
CLK_COM1	Chip * 128	((Chip+1) * 128) -1
CLK_ERROR	Chip * 128	((Chip+1) * 128) -1

RAW DATA:

ABCD_CONFIG (optional)

Acceptance

None of the defects found by this test are allowable on production modules, hence the “PASS” field will be set to “NO” if any defects are found.

Sample Output from the Results File

```
#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY  : pwp
LOCATION NAME   : RAL
Run number    : 256-7
TEST_DATE     : 09/08/2001
PASSED        : YES
PROBLEM       : NO
#
%DAQ_INFO
#
#HOST
"HEPNTW124"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"18:15:18"
#
%DCS_INFO
#
#T0      T1
25.5     26.3
#VDET    IDET
350      1.220
#VCC     ICC
3.500    790
#VDD     IDD
4.000    535
#
%RedundancyTest
#
#RedundancyTest Summary - not for the database
#chip pass good stuck dead adr0 adr1 com0 com1 com
# 0 1 128 0 0 0 0 0 0 0 0
# 1 1 128 0 0 0 0 0 0 0 0
# 2 1 128 0 0 0 0 0 0 0 0
# 3 1 128 0 0 0 0 0 0 0 0
# 4 1 128 0 0 0 0 0 0 0 0
# 5 1 128 0 0 0 0 0 0 0 0
# 6 1 128 0 0 0 0 0 0 0 0
# 7 1 128 0 0 0 0 0 0 0 0
# 8 1 128 0 0 0 0 0 0 0 0
# 9 1 128 0 0 0 0 0 0 0 0
#10 1 128 0 0 0 0 0 0 0 0
#11 1 128 0 0 0 0 0 0 0 0
#
#No defects found!
#
#No raw data!
```

FullBypassTest.cpp

The module is programmed to each possible configuration with regard to the routing of token and data between the chips. Since the irradiation programme has shown that different chips can have different susceptibilities to radiation damage effects with regard to the token passing, this test is performed over a range of digital voltages, Vdd. In this way the minimum value of Vdd required for the correct operation of each bypass link can be determined, and any inherent difference in the performance of the various links is known upon production.

The number of configurations to be tested is greater for forward hybrids than for barrel hybrids since more redundancy links have been implemented in the forward design.

Method

SETTINGS	Configuration	Master/Slave/End	(variable) SEE BELOW
		Edge Detect	OFF
		Data Compression	X1X
		Mode	MASK + Data Taking Mode
		Select	0
		Masked Channels	None
	DACs	Ipreamp	220µA
		Ishaper	30µA
		Threshold DAC	500mV
		Calibration DAC	10mV (1.0fC)
		Delay Register	-
		TrimRange	0
		TrimDAC	0
	TRIGGER	Sequence	L1A
Frequency		-	
SCANS	LOOPS	1 – Vdd	4.0, 3.9, 3.8, 3.7, 3.6, 3.5
		2 – Configuration	Barrel hybrid or module: cases 0 – 35 Forward hybrid or module: cases 0 – 62
	n Triggers		100

Analysis

For each configuration, the number of dead channels of each chip is tallied. Chips having more than 120 dead channels are considered to have returned no data, otherwise they are considered to have returned good data. This matrix is then compared with expectation to determine the minimum value of Vdd needed for the correct operation of each bypass link.

Any bypass links that do not function correctly when Vdd is set to the minimum value of 3.5V are recorded as DEFECTS. In this case Vdd_min is recorded as 10.0V. In the case where a link has not been tested, Vdd_min is recorded as 0V. A comment is recorded in each case.

Database

The following information should be stored in the SCT database:

<u>TSTDAQINFO:</u>	host and version information
<u>TSTDCSINFO:</u>	monitored voltages, currents and temperatures
<u>TSTHYBBPASS:</u>	minimum Vdd required for operation of each token/bypass link

DEFECTS:

Defect	First Chan	Last Chan
TOKEN	Chip * 128	((Chip+1) * 128) -1
RTOKEN	Chip * 128	((Chip+1) * 128) -1

RAW DATA:

ABCD_CONFIG (optional)

Acceptance

A global "PASS" will be recorded if no defects are found.

Sample Output from the Results File

```
#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY : pwp
LOCATION NAME : RAL
Run number : 256-7
TEST_DATE : 09/08/2001
PASSED : YES
PROBLEM : NO
#
%DAQ_INFO
#
#HOST
"HEPNTW124"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"18:15:06"
#
%DCS_INFO
#
#T0 T1
25.5 26.3
#VDET IDET
350 1.220
#VCC ICC
3.500 790
#VDD IDD
4.000 535
#
%FullBypassTest
#
#Vmin
#token r_tkn token r_tkn
#M0 S1
3.5 3.5 3.5 3.5
#S2 S3
3.5 3.5 3.5 3.5
#S4 E5
3.5 0.0 0.0 3.5
#M8 S9
3.5 3.5 3.5 3.5
#S10 S11
3.5 3.5 3.5 3.5
#S12 #E13
3.5 0.0 0.0 3.5
#
```

```

#Comment
#token r_tkn token r_tkn
#M0 S1
"Minimal tested" "Minimal tested" "Minimal tested" "Minimal tested"
#S2 #S3
"Minimal tested" "Minimal tested" "Minimal tested" "Minimal tested"
#S4 #E5
"Minimal tested" "Not tested" "Not tested" "Minimal tested"
#M8 #S9
"Minimal tested" "Minimal tested" "Minimal tested" "Minimal tested"
#S10 S11
"Minimal tested" "Minimal tested" "Minimal tested" "Minimal tested"
#S12 E13
"Minimal tested" "Not tested" "Not tested" "Minimal tested"
#
%DEFECTS
#name bypass_link Vdd_min
#No defects found!

```

PipelineTest.cpp

The cells of the ABCD3T pipeline are tested in order to identify any cells which may permanently output zero (dead) or one (stuck). (Although the pipeline has already been tested during wafer probing, it may be desired to repeat this test to identify any new failures.) The pulse input register facility is also tested.

Method

	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E	
		SETTINGS	Edge Detect	OFF											
Data Compression	X1X														
Mode	Data Taking Mode														
Select	0														
Masked Channels	None														
DACs	Ipreamp		220µA												
	Ishaper		30µA												
	Threshold DAC		500mV												
	Calibration DAC		10mV (1.0fC)												
	Delay Register		-												
	TrimRange		0												
TRIGGER	TrimDAC		0												
	Sequence		Soft Reset + n BCO delay + Pulse Input Register Command + 129 BCO delay + L1A												
	Frequency		-												
SCANS	LOOPS	1 – MASK	Mask #0, #3												
		2 – n BCO delay	150 to 161, step size = 1												
	n Triggers	100													

The mask patterns to be used are as follows:

1. no channels masked (to identify dead cells)
3. all channels masked (to identify stuck cells)

Analysis

The number of channels that return data for each scanpoint is tallied – corresponding to the number of good channels. If for a given channel all 12 cells are found to be dead or stuck, then a defect type of DEADⁱⁱⁱ or STUCK is recorded. If for any channel the number of dead cells or stuck cells is greater than zero but less than 12, each individual defect is noted as either type DEADCELL or STUCKCELL.

Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures
TSTHYBPIPE: the number of good pipeline cells in each chip

DEFECTS:

Defect	First Chan	Last Chan
DEAD	CHANNEL	CHANNEL
STUCK	CHANNEL	CHANNEL
DEADCELL	CHANNEL	CHANNEL
STUCKCELL	CHANNEL	CHANNEL

RAW DATA:

ABCD_CONFIG (optional)

Acceptance

None of the defects found by this test are allowable on production modules, hence the “PASS” field will be set to “NO” if any defects were found.

ⁱⁱⁱ In the event that this test finds a channel to be dead, a fault in the mask register would be one possible cause. In combination with the data set from the Redundancy Test it would be possible to identify dead cells in the mask register – but this seems excessive.

Sample Output from the Results File

```
#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY : pwp
LOCATION NAME : RAL
Run number : 256-8
TEST_DATE : 09/08/2001
PASSED : YES
PROBLEM : NO
#
%DAQ_INFO
#
#HOST
"HEPNTWL24"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"18:15:25"
#
%DCS_INFO
#
#T0 T2
25.5 26.3
#VDET IDET
350 1.220
#VCC ICC
3.500 790
#VDD IDD
4.000 535
#
%PipelineTest
#
#NGOOD
#M0 S1 S2 S3 S4 E5
128 128 128 128 128 128
#
#M8 S9 S10 S11 S12 E13
128 128 128 128 128 128
#
#No defects found!
#
#No raw data!
```

Description of Analogue Tests

StrobeDelay.cpp

This test aims to establish the optimum setting of the delay register for each chip, to be used during all subsequent analogue tests. The size of each delay step is known to vary as a function of temperature, hence the strobe delay setting must always be re-optimised each time a device is operated at a different temperature. Sufficient time must always be allowed for the powered, configured hybrid or module to reach thermal equilibrium with its surroundings before this test may be undertaken.

Running with Edge Detect ON, compression 01X, a 4.0fC signal is injected for a threshold of 2.0fC. A functional fit is made to both the rising and falling edges to give the points at which 50% efficiency is achieved. The operating point is chosen to be 25% of the distance between these two points with reference to the rising edge of the strobe delay peak, which corresponds to the falling edge of the signal. By setting the timing some distance behind this edge, good efficiency can be ensured even for small signals. (This method gives answers in close agreement with a point 20% of the way along the plateau for a module of typically 1450 ENC noise.)

Method

The macro first performs a threshold scan with 2fC injected charge and set the threshold of each chip in accordance with the calculated mean VT50 values. Next the actual delay scan is performed as described below:

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E	
		Edge Detect	ON												
		Data Compression	01X												
		Mode	Data Taking Mode												
		Select	0												
		Masked Channels	None												
	DACs	Ipreamp	220µA												
		Ishaper	30µA												
		Threshold DAC	(2.0fC)												
		Calibration DAC	40mV (4.0fC)												
		Delay Register	(scanned)												
		TrimRange	0												
		TrimDAC	0												
	TRIGGER	Sequence	Calibration Pulse + 131 BCO delay + L1A												
		Frequency	-												
SCANS	LOOPS	1 – Delay	0 to 63, step size = 1												
	N Triggers	1000													

Analysis

The analysis as described below is repeated for each chip in turn.

An error function is fitted to the rising edge of a strobe delay peak, corresponding to the falling edge of the signal. Similarly a complementary error function is fitted to the falling edge, corresponding to the rising edge of the signal. The width of the strobe delay peak is now known and the strobe delay register is set to a point 25% of the distance between the two edges, such that the electronics remain efficient for smaller signals.

If the fit to the rising edge of the strobe delay peak returns a value below the permitted minimum of 0 or the fit to the falling edge returns a value above the permitted minimum of 35, the defect SD_LO is recorded. Similarly if the fit to the falling edge of the strobe delay peak returns a value above the permitted maximum of 28 or the fit to the falling edge returns a value above the permitted maximum of 63, the defect SD_HI is recorded.

Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures
TSTHYBDELAY: Strobe delay setting for each chip

DEFECTS:

Defect	First Channel	Last Channel
SD_LO	Chip * 128	((Chip+1) * 128) -1
SD_HI	Chip * 128	((Chip+1) * 128) -1

RAW DATA:

ABCD_CONFIG (optional)

Acceptance

None of the defects found by this test are allowable on production modules, hence the “PASS” field will be set to “NO” if any defects were found.

The database reporting structure should also provide the possibility to set acceptance cuts on the range of delay values.

Sample Output from the Results File

```
#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY  : pwp
LOCATION NAME   : RAL
Run number    : 256-11
TEST_DATE     : 09/08/2001
PASSED        : YES
PROBLEM       : NO
#
%DAQ_INFO
#
#HOST
"HEPNTWL24"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"18:17:13"
#
%DCS_INFO
#
#T0      T1
25.5     26.3
#VDET    IDET
350      1.220
#VCC     ICC
3.500    790
#VDD     IDD
4.000    535
#
%StrobeDelay
#
#DELAY
#M0 S1  S2  S3  S4  E5
-1  -1  -1  -1  16  17
#
#M8 S9  S10 S11 S12 E13
17  15  16  16  16  18
#
%Defect
DEFECT NAME : SD_LO
FIRST CHANNEL : 0
LAST CHANNEL : 127
#
%Defect
DEFECT NAME : SD_LO
FIRST CHANNEL : 128
LAST CHANNEL : 255
#
%Defect
DEFECT NAME : SD_LO
FIRST CHANNEL : 256
LAST CHANNEL : 383
#
%Defect
DEFECT NAME : SD_LO
FIRST CHANNEL : 384
LAST CHANNEL : 511
#
#4 defects found
#
#No raw data!
```

ThreePointGain.cpp

Threshold scans are taken for three injected charges to facilitate a quick measurement of gain and noise and to give an estimation of the discriminator offset. Notably in the case of a module, threshold scans taken with small charges (<1.5fC) yield s-curves which are distorted at low thresholds due to noise occupancy. Fitting the complementary error function to such an s-curve, the noise is under estimated. For this reason, it is best to make noise measurements with injected charges of 1.5fC or more.

Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E	
		Edge Detect	OFF												
		Data Compression	X1X												
		Mode	Data Taking Mode												
		Select	0												
		Masked Channels	None												
	DACs	Ipreamp	220µA												
		Ishaper	30µA												
		Threshold DAC	(scanned)												
		Calibration DAC	(variable)												
		Delay Register	(optimised)												
		TrimRange	0												
		TrimDAC	(trimmed or untrimmed as appropriate)												
	TRIGGER	Sequence	Calibration Pulse + 131 BCO delay + L1A												
Frequency		-													
SCANS	LOOPS	1 – Qinj	1.50fC, 2.00fC, 2.50fC												
		2 – THRESHOLD	Ranges and step sizes to be determined												
		3 – CAL LINE	0, 1, 2, 3												
	n Triggers	1000													

Analysis

A complementary error function is fitted to each threshold scan to yield values of VT50 and output noise for each channel. A straight line is fitted to each set of three VT50 points to determine the gain and offset of each channel. The input noise can now be calculated by dividing the output noise measured at 2fC by the calculated gain.

Anomalous channels are categorised as follows:

Defect	Condition	Default value of cut
DEAD	No output	-
STUCK	Continuous output	-
LO_GAIN	Gain < MIN_GAIN	0 (mV/fC)
HI_GAIN	Gain > MAX_GAIN	100 (mV/fC)
LO_OFFSET	Offset < MIN_OFFSET	-100 (mV)
HI_OFFSET	Offset > MAX_OFFSET	120 (mV)
UNBONDED	Noise < BONDED_NOISE	750 (ENC)
PARTBONDED	Noise < MIN_INNSE	1100 (ENC)
NOISY	Noise > (mean_noise + (3* rms_noise))	-
INEFFICIENT	Maximum efficiency <100%	(not yet implemented)

Database

The following information should be stored in the SCT database:

<u>TSTDAQINFO:</u>	host and version information
<u>TSTDCSINFO:</u>	monitored voltages, currents and temperatures
<u>TSTSCANINFO:</u>	number of scan points and corresponding charge values
<u>TSTHYBRC:</u>	response curve, gain, noise and offset information

DEFECTS:

Defect	First Channel	Last Channel
DEAD	First Channel	Last Channel
STUCK	First Channel	Last Channel
LO_GAIN	First Channel	Last Channel
HI_GAIN	First Channel	Last Channel
LO_OFFSET	First Channel	Last Channel
HI_OFFSET	First Channel	Last Channel
UNBONDED	First Channel	Last Channel
PARTBONDED	First Channel	Last Channel
NOISY	First Channel	Last Channel
INEFF	First Channel	Last Channel

RAW DATA:

ABCD_CONFIG (optional)
CHANNEL_DATA (mandatory)

Acceptance

Use of the "PASS" field has not been implemented for this test, it is always set to be "YES".

The database reporting structure must provide the possibility to set acceptance cuts on the mean and rms of VT50, gain, offset and noise, together with cuts on the maximum number of allowable channel defects falling into each of the following two categories:

- A) LOST DEAD, STUCK, UNBONDED, NOISY
- B) FAULTY LO_GAIN, HI_GAIN, LO_OFFSET, HI_OFFSET,
PARTBONDED, INEFFICIENT

Sample Output from the Results File

```
#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY  : pwp
LOCATION NAME   : RAL
Run number    : 256-12
TEST_DATE     : 09/08/2001
PASSED        : YES
PROBLEM       : NO
#
%DAQ_INFO
#
#HOST
"HEPNTW124"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"18:19:21"
#
%DCS_INFO
#
#T0      T1
25.5     26.3
#VDET    IDET
350      1.220
#VCC     ICC
3.500    790
#VDD     IDD
4.000    535
#
%SCAN_INFO
#
#POINT TYPE
"QCAL (fC)"
#N_POINTS
3
#POINTS
1.50     2.00     2.50
#
%ThreePointGain
#
#Loop A - Fit
#      func    p0      p1      p2
#M0      4      0.00    0.00    0.00
#S1      4      0.00    0.00    0.00
#S2      4      0.00    0.00    0.00
#S3      4      0.00    0.00    0.00
#S4      4      0.00    0.00    0.00
#E5      4      6.86    59.97   0.00
#M8      4      6.65    60.45   0.00
#S9      4      12.97   55.31   0.00
#S10     4      11.82   55.19   0.00
#S11     4      9.11    57.38   0.00
#S12     4      8.23    53.75   0.00
#E13     4      11.84   55.00   0.00
#      4      10.72   60.70   0.00
#
```

```

#Loop B - Gain, Offset, Noise at 2.00fC
# vt50 rms gain rms offset rms outnse innse rms
#M0 0.0 0.00 0.0 0.00 0.0 0.00 0.00 0 0
#S1 0.0 0.00 0.0 0.00 0.0 0.00 0.00 0 0
#S2 0.0 0.00 0.0 0.00 0.0 0.00 0.00 0 0
#S3 0.0 0.00 0.0 0.00 0.0 0.00 0.00 0 0
#S4 127.2 8.58 60.0 1.40 9.6 6.02 14.00 1460 29
#S5 128.7 7.55 60.4 1.36 8.1 4.95 12.90 1336 32
#M8 123.8 8.64 55.3 1.21 13.9 7.60 13.68 1546 79
#S9 122.5 10.16 55.2 1.04 14.4 7.49 13.49 1528 40
#S10 124.6 10.09 57.4 1.24 12.0 7.67 13.71 1494 34
#S11 115.9 9.68 53.8 1.13 10.8 7.36 12.93 1504 35
#S12 121.8 9.32 55.0 1.24 12.8 7.77 13.31 1513 116
#E13 132.5 7.63 60.7 1.04 11.8 6.29 13.59 1400 34
#
#Loop C - comment
#M0 S1 S2 S3 S4 E5
"dead" "dead" "dead" "dead" "OK" "OK"
#M8 S9 S10 S11 S12 E13
"OK" "OK" "OK" "OK" "OK" "OK"
#
%Defect
DEFECT NAME : DEAD
FIRST CHANNEL : 0
LAST CHANNEL : 511
#
%Defect
DEFECT NAME : PARTBONDED
FIRST CHANNEL : 768
LAST CHANNEL : 768
#
%Defect
DEFECT NAME : PARTBONDED
FIRST CHANNEL : 774
LAST CHANNEL : 774
#
%Defect
DEFECT NAME : UNBONDED
FIRST CHANNEL : 1391
LAST CHANNEL : 1391
#
%Defect
DEFECT NAME : UNBONDED
FIRST CHANNEL : 1393
LAST CHANNEL : 1393
#
#5 defects found
#
%TEST Rawdata
FILENAME : D:\sctvar\results\20220170100016_rc_246-12.txt

```

TrimRange.cpp

During production, the chips used to build modules will be selected such that the offsets of all channels may be brought into line by adjustment of the TrimDAC using the minimum step size (TrimRange). In ATLAS it will be necessary to increase the size of each TrimDAC in order to accommodate the increase in the offset spread as a function of radiation dose. Hence it is necessary to determine the initial TrimDAC characteristic for each of the four TrimRange settings.

For TrimRange 0, the TrimDAC characteristic is studied using each of the possible TrimDAC values. This is done to ensure that each step may be selected and to demonstrate that the TrimDAC characteristic is linear and monotonic for all steps. For the remaining three TrimRange settings, the TrimDAC characteristic is studied using only 4 of the possible TrimDAC values. The prime motivation for this reduction in the number of component scans is to save time during testing.

Since the nominal operating threshold in ATLAS will be 1.0fC, the TrimDAC/TrimRange characterisation should be performed in response to 1.0fC injected charge.

Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E	
		Edge Detect													OFF
		Data Compression													X1X
		Mode													Data Taking Mode
		Select													0
		Masked Channels													None
	DACs	Ipreamp													220 μ A
		Ishaper													30 μ A
		Threshold DAC													(scanned)
		Calibration DAC													10mV (1.0fC)
		Delay Register													(optimised)
		TrimRange													(scanned)
		TrimDAC													(scanned)
	TRIGGER	Sequence													Calibration Pulse + 131 BCO delay + L1A
Frequency														-	
SCANS	LOOPS	1 – Trim Range													0 to 4, step size = 1
		2 – TrimDAC													TR=0:(0 to 15) TR=1,2,3: (3, 7, 11, 15)
		3 – THRESHOLD													Ranges and step sizes to be determined
		4 – CAL LINE													0, 1, 2, 3
	n Triggers													200	

Analysis

Each scan is fitted in turn to yield a matrix giving the threshold needed to obtain 50% efficiency (VT50) for 1fC input charge as a function of TrimDAC setting. For each combination of TrimRange and channel number, a straight line is fitted to the data to determine the step size and offset of the corresponding TrimDAC characteristic. Any points for which the s-curve fitting returned an error are ignored but the present version of the code does not include a noise cut at this stage.

For each TrimRange, a range of targets (2.5mV to 300mV in 2.5mV steps) is studied to determine the maximum number of channels that can be brought into line. For each channel in turn, the fitted TrimDAC characteristic is solved to determine the TrimDAC setting needed to reach the studied targets. If the calculated value is within the range of possible TrimDAC settings, the channel is considered to be trimmable for that combination of TrimRange and target.

At a second pass, the TrimRange value for each chip is chosen to maximise the number of trimmable channels. By default this is done such that all channels of the module are trimmed to the same target value, but the option exists to allow each chip to be trimmed to a different target.

For each TrimRange setting, an ASCII file is generated listing the TrimDAC values for each chip. For historical reasons this takes the form of a floating point number between 0 and 1, but this may change to a more logical format such as an integer between 0 and 15. A fifth trim file is generated listing the TrimRange and TrimDAC settings found to be best overall for the hybrid or module under test.

In each of the above five cases a corresponding mask file is generated listing those channels to be masked and the reasons why. In addition to untrimmable channels, dead, stuck and particularly noisy channels are also masked. (In this instance a particularly noisy channel is defined to be one with output noise more than 125% the mean output noise of the parent chip.)

Defective chips and/or channels are categorised as follows:

Defect	Description	Condition(s)
TR_RANGE	A chip for which the mean step size is not as expected for the presently selected TrimRange	TR0: step < 1.5 or step > 5.0 ^{iv} TR1: step < 5.0 or step > 8.5 TR2: step < 8.5 or step > 12.0 TR3: step < 12.0 or step > 15.5
TR_STEP	A channel for which the step size differs from the mean step size of that chip	Step < (mn_step - (3* rms_step)) Step > (mn_step + (3* rms_step))
TR_OFFSET	A channel for which the offset differs from the mean offset of that chip	Offset < (mn_offset - (3* rms_offset)) Offset > (mn_offset + (3* rms_offset))

Database

The results of this test should be stored in the SCT database using five instances of the following table, with TRIM_TYPE = {0,1,2,3,-1} corresponding to TrimRange=0, TrimRange=1, TrimRange=2, TrimRange=3, and with optimised TrimRange settings. In each case the trim and mask files should be uploaded to the database for future reference.

<u>TSTDAQINFO:</u>	host and version information
<u>TSTDCSINFO:</u>	monitored voltages, currents and temperatures
<u>TSTSCANINFO:</u>	number of scans and corresponding TrimDAC settings
<u>TSTHYBTRIM:</u>	trim summary

DEFECTS:

Defect	First Channel	Last Channel
TR_RANGE	Chip * 128	((Chip+1) *128)-1
TR_STEP	First Channel	Last Channel
TR_OFFSET	First Channel	Last Channel

RAW DATA:

ABCD_CONFIG (optional)
TRIM_DATA (mandatory)

Acceptance

The “PASS” field is set to “NO” if any defect of type TR_RANGE has been recorded.

The database reporting structure should also provide the possibility to set acceptance cuts on the number of trimmable channels, the mean and rms of the distribution of vt50 values after trimming, the TrimDAC offset and the TrimDAC step size.

^{iv} These cuts are provisional, and may change with future batches of ABCD3T wafers.

Sample Output from the Results File

Example 1: with all chips set to TrimRange 0

```
#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY : pwp
LOCATION NAME : RAL
Run number : 256-15
TEST_DATE : 09/08/2001
PASSED : YES
PROBLEM : NO
#
%DAQ_INFO
#
#HOST
"HEPNTW124"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"18:52:39"
#
%DCS_INFO
#
#T0 T1
25.5 26.3
#VDET IDET
350 1.220
#VCC ICC
3.500 790
#VDD IDD
4.000 535
#
%SCAN_INFO
%
#POINT TYPE
"TrimDAC (bits)"
#N_POINTS
16
#POINTS
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
#
```

```

%Trim
#
#TRIM  CHARGE  TYPE  ALGORITHM
      10.0    0      0
#(trim whole module)
#
#      range  target  ntrim  vt50   vt50rms  tr_off  off_rms  tr_step  step_rms
#M0    0      87.5   0      0.0    0.00    0.0    0.0    0.00    0.00
#S1    0      87.5   0      0.0    0.00    0.0    0.0    0.00    0.00
#S2    0      87.5   0      0.0    0.00    0.0    0.0    0.00    0.00
#S3    0      87.5   0      0.0    0.00    0.0    0.0    0.00    0.00
#S4    0      87.5   0      0.0    0.00    0.0    0.0    0.00    0.00
#E5    0      87.5  128    86.8   1.18   -20.2   2.5    3.33    0.15
#M8    0      87.5  128    86.9   1.23   -19.1   1.9    3.62    0.20
#S9    0      87.5  128    87.1   1.05   -19.6   2.4    3.47    0.17
#S10   0      87.5  128    86.9   1.12   -19.3   2.8    3.48    0.16
#S11   0      87.5  128    87.1   1.14   -22.6   3.3    2.99    0.15
#S12   0      87.5  128    86.9   1.05   -19.1   3.0    3.24    0.19
#E13   0      87.5  128    87.1   1.10   -20.4   2.7    3.27    0.21
#E13   0      87.5  127    86.9   1.27   -19.0   2.1    3.79    0.20
#
%DEFECTS
#name  channel value
%Defect
DEFECT NAME   : TR_RANGE
FIRST CHANNEL : 0
LAST CHANNEL  : 127
#
%Defect
DEFECT NAME   : TR_RANGE
FIRST CHANNEL : 128
LAST CHANNEL  : 255
#
%Defect
DEFECT NAME   : TR_RANGE
FIRST CHANNEL : 256
LAST CHANNEL  : 383
#
%Defect
DEFECT NAME   : TR_RANGE
FIRST CHANNEL : 384
LAST CHANNEL  : 512
#
%Defect
DEFECT NAME   : TR_STEP
FIRST CHANNEL : 636
LAST CHANNEL  : 636
#
%Defect
DEFECT NAME   : TR_STEP
FIRST CHANNEL : 639
LAST CHANNEL  : 639
#
%Defect
DEFECT NAME   : TR_STEP
FIRST CHANNEL : 895
LAST CHANNEL  : 895
#
%Defect
DEFECT NAME   : TR_STEP
FIRST CHANNEL : 1019
LAST CHANNEL  : 1019
#

```

```

%Defect
DEFECT NAME      : TR_STEP
FIRST CHANNEL    : 1151
LAST CHANNEL     : 1151
#
%Defect
DEFECT NAME      : TR_STEP
FIRST CHANNEL    : 721
LAST CHANNEL     : 721
#
#10 defects found
#
%TEST Rawdata
FILENAME         D:\sctvar\results\20220170100016_tr0_20010824.trim

```

Example 2: with optimised TrimRange settings

```

#
%NEW_TEST
#
SERIAL NUMBER    : 20220170100016
TEST MADE BY     : pwp
LOCATION NAME      : RAL
Run number       : 256-15
TEST_DATE        : 09/08/2001
PASSED           : YES
PROBLEM          : NO
#
%DAQ_INFO
#
#HOST
"HEPNTW124"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"18:52:39"
#
%DCS_INFO
#
#T0      T1
25.5     26.3
#VDET    IDET
350      1.220
#VCC     ICC
3.500    790
#VDD     IDD
4.000    535
#
%Trim
%
#TRIM    CHARGE  TYPE    ALGORITHM
         10.0    -1      0
#(trim whole module)
#
TRIM_FILE      D:\sctvar\results\20220170100016_tr-1_20010824.trim
#
#         range  target  ntrim  vt50   vt50rms tr_off  off_rms tr_step step_rms
#M0
#S1
#S2
#S3
#S4
#E5
#M8
#S9
#S10

```

	range	target	ntrim	vt50	vt50rms	tr_off	off_rms	tr_step	step_rms
#M0	0	87.5	0	0.0	0.00	0.0	0.0	0.00	0.00
#S1	0	87.5	0	0.0	0.00	0.0	0.0	0.00	0.00
#S2	0	87.5	0	0.0	0.00	0.0	0.0	0.00	0.00
#S3	0	87.5	0	0.0	0.00	0.0	0.0	0.00	0.00
#S4	87.5	128	86.9	0.96	-20.2	2.5	3.33	0.15	
#E5	87.5	128	87.1	1.03	-19.1	1.9	3.62	0.20	
#M8	87.5	128	87.2	0.92	-19.6	2.4	3.47	0.17	
#S9	87.5	128	87.0	0.97	-19.3	2.8	3.48	0.16	
#S10	7.5	128	87.1	1.00	-22.6	3.3	2.99	0.15	

```

#S11      7.5    128    86.8    0.96   -19.1    3.0    3.24    0.19
#S12      7.5    128    87.1    0.97   -20.4    2.7    3.27    0.21
#E13      7.5    128    87.2    2.22   -9.7     1.1    7.37    0.36
#
%DEFECTS
#name  channel value
%Defect
DEFECT NAME      : TR_RANGE
FIRST CHANNEL    : 0
LAST CHANNEL     : 127
#
%Defect
DEFECT NAME      : TR_RANGE
FIRST CHANNEL    : 128
LAST CHANNEL     : 255
#
%Defect
DEFECT NAME      : TR_RANGE
FIRST CHANNEL    : 256
LAST CHANNEL     : 383
#
%Defect
DEFECT NAME      : TR_RANGE
FIRST CHANNEL    : 384
LAST CHANNEL     : 512
#
%Defect
DEFECT NAME      : TR_STEP
FIRST CHANNEL    : 636
LAST CHANNEL     : 636
#
%Defect
DEFECT NAME      : TR_STEP
FIRST CHANNEL    : 639
LAST CHANNEL     : 639
#
%Defect
DEFECT NAME      : TR_STEP
FIRST CHANNEL    : 895
LAST CHANNEL     : 895
#
%Defect
DEFECT NAME      : TR_STEP
FIRST CHANNEL    : 1019
LAST CHANNEL     : 1019
#
%Defect
DEFECT NAME      : TR_STEP
FIRST CHANNEL    : 1151
LAST CHANNEL     : 1151
#
%Defect
DEFECT NAME      : TR_STEP
FIRST CHANNEL    : 721
LAST CHANNEL     : 721
#
#10 defects found
#
%TEST Rawdata
FILENAME          D:\sctvar\results\20220170100016_tr-1_20010824.trim

```

ResponseCurve.cpp

Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E	
		Edge Detect	OFF ^v												
		Data Compression	X1X												
		Mode	Data Taking Mode												
		Select	0												
		Masked Channels	Untrimmable, Stuck, Dead and Noisy Channels												
	DACs	Ipreamp	220 μ A												
		Ishaper	30 μ A												
		Threshold DAC	(scanned)												
		Calibration DAC	(variable)												
		Delay Register	(optimised)												
		TrimRange	0												
		TrimDAC	(optimised)												
	TRIGGER	Sequence	Calibration Pulse + 131 BCO delay + L1A												
Frequency		-													
SCANS	LOOPS	1 – Qinj	0.50fC, 0.75fC, 1.00fC, 1.25fC, 1.50fC, 2.00fC, 3.00fC, 4.00fC, 6.00fC, 8.00fC												
		2 – THRESHOLD	Ranges and step sizes to be determined												
		3 – CAL LINE	0, 1, 2, 3												
	n Triggers	1000													

Analysis

A complementary error function is fitted to each threshold scan to yield values of VT50 and output noise for each channel. A straight line is fitted to each set of three VT50 points to determine the gain and offset of each channel. The input noise can now be calculated by dividing the output noise measured at 2fC by the calculated gain.

Anomalous channels are categorised as follows:

Defect	Condition	Default value of cut
DEAD	No output	-
STUCK	Continuous output	-
LO_GAIN	Gain < MIN_GAIN	0 (mV/fC)
HI_GAIN	Gain > MAX_GAIN	100 (mV/fC)
LO_OFFSET	Offset < MIN_OFFSET	-100 (mV)
HI_OFFSET	Offset > MAX_OFFSET	120 (mV)
UNBONDED	Noise < BONDED_NOISE	750 (ENC)
PARTBONDED	Noise < MIN_INNSE	1100 (ENC)
NOISY	Noise > (mean_noise + (3* rms_noise))	-
INEFFICIENT	Maximum efficiency <100%	(not yet implemented)

Database

This test has the same inputs and outputs as [ThreePointGain.cpp](#):

TSTDAQINFO:	host and version information
TSTDCSINFO:	monitored voltages, currents and temperatures
TSTSCANINFO:	number of scan points and corresponding charge values
TSTHYBRC:	response curve, gain, noise and offset information

^v When running with EDGE DETECT ON / EDGE COMPRESSION, threshold scans with small charges do not reach 100% efficiency since the noise is of comparable value to the injected charge. By running with edge detect off, in any other compression mode, such problems are minimised.

DEFECTS:

Defect	First Channel	Last Channel
DEAD	First Channel	Last Channel
STUCK	First Channel	Last Channel
LO_GAIN	First Channel	Last Channel
HI_GAIN	First Channel	Last Channel
LO_OFFSET	First Channel	Last Channel
HI_OFFSET	First Channel	Last Channel
UNBONDED	First Channel	Last Channel
PARTBONDED	First Channel	Last Channel
NOISY	First Channel	Last Channel
INEFF	First Channel	Last Channel

RAW DATA:

ABCD_CONFIG (optional)

CHANNEL_DATA (mandatory)

Acceptance

Use of the "PASS" field has not been implemented for this test, it is always set to be "YES".

The database reporting structure must provide the possibility to set acceptance cuts on the mean and rms of VT50, gain, offset and noise, together with cuts on the maximum number of allowable channel defects falling into each of the following two categories:

- A) LOST DEAD, STUCK, UNBONDED, NOISY
- B) FAULTY LO_GAIN, HI_GAIN, LO_OFFSET, HI_OFFSET,
PARTBONDED, INEFFICIENT

Sample Output from the Results File

```

#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY  : pwp
LOCATION NAME   : RAL
Run number    : 256-43
TEST_DATE     : 09/08/2001
PASSED        : YES
PROBLEM       : NO
#
%DAQ_INFO
#
#HOST
"HEPNTWL24"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"18:41:55"
#
%DCS_INFO
#
#T0      T1
25.5     26.3
#VDET    IDET
350      1.220
#VCC     ICC
3.500    790
#VDD     IDD
4.000    535
#
%SCAN_INFO
#
#POINT TYPE
"QCAL (fC)"
#N_POINTS
10
#POINTS
0.50    0.75    1.00    1.25    1.50    2.00    3.00    4.00
6.00    8.00
#
%ResponseCurve
#
#Loop A - Fit
#      func    p0      p1      p2
#M0      3      0.01    46.01   -0.00
#S1      3      0.01    46.01   -0.00
#S2      3      0.01    46.01   -0.00
#S3      3      0.01    46.01   -0.00
#S4      3      0.01    46.01   -0.00
#S5      3      1571.96 6.63    -757.75
#E5      3      1572.40 6.71    -757.43
#M8      3      1676.52 7.59    -805.92
#S9      3      1613.51 7.35    -774.31
#S10     3      1659.59 7.37    -798.54
#S11     3      1802.85 8.44    -867.39
#S12     3      1716.86 7.78    -826.15
#E13     3      1637.46 6.78    -791.18
#

```

```

#Loop B - Gain, Offset, Noise at 2.00fC
# vt50 rms gain rms offset rms outnse innse rms
#M0 0.0 0.00 0.0 0.00 0.0 0.00 0.00 0 0
#S1 0.0 0.00 0.0 0.00 0.0 0.00 0.00 0 0
#S2 0.0 0.00 0.0 0.00 0.0 0.00 0.00 0 0
#S3 0.0 0.00 0.0 0.00 0.0 0.00 0.00 0 0
#S4 146.6 1.80 57.8 1.42 28.6 1.91 13.82 1494 34
#E5 146.9 1.72 57.3 1.05 28.9 1.54 13.23 1443 35
#M8 142.1 1.62 54.2 1.25 32.5 1.69 13.39 1545 76
#S9 141.7 1.38 53.7 1.11 32.8 1.83 13.33 1553 40
#S10 144.0 1.50 55.2 1.20 31.4 1.71 13.70 1550 34
#S11 140.3 1.42 52.4 1.10 34.4 1.73 12.97 1546 30
#S12 141.6 1.49 54.0 1.24 32.7 1.92 13.40 1551 120
#E13 147.9 2.51 58.9 0.93 27.9 2.66 13.77 1463 37
#
#Loop C - comment
#M0 S1 S2 S3 S4 E5
"dead" "dead" "dead" "dead" "OK" "OK"
#M8 S9 S10 S11 S12 E13
"OK" "OK" "OK" "OK" "OK" "OK"
#
%Defect
DEFECT NAME : DEAD
FIRST CHANNEL : 0
LAST CHANNEL : 511
#
%Defect
DEFECT NAME : PARTBONDED
FIRST CHANNEL : 768
LAST CHANNEL : 768
#
%Defect
DEFECT NAME : PARTBONDED
FIRST CHANNEL : 774
LAST CHANNEL : 774
#
%Defect
DEFECT NAME : UNBONDED
FIRST CHANNEL : 1391
LAST CHANNEL : 1391
#
%Defect
DEFECT NAME : UNBONDED
FIRST CHANNEL : 1393
LAST CHANNEL : 1393
#
#5 defects found
#
%TEST Rawdata
FILENAME : D:\sctvar\results\20220170100016_rc_246-43.txt

```

NO.cpp

For this measurement, the trigger frequency should approach the nominal ATLAS trigger rate of 100kHz^{vi}, being throttled back as necessary at higher occupancies in order to avoid buffer overflow errors. In order to measure noise occupancies down to the level of 10^{-6} up to 10^6 events are taken. At the other end of the scale, where occupancy approaches 1.0, only 2000 events are recorded. Between the two extremes the fractional occupancy of each channel is calculated after each partial burst and the number of events taken is varied such that, for each scanpoint, a minimum of 50 hits are seen in more than 50% of the active readout channels. In the case that the occupancy of a given channel should overflow the depth of the MuSTARD histogram memory, its fractional occupancy is frozen as that determined prior to the overflow condition.

Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E
		Edge Detect	OFF											
		Data Compression	X1X											
		Mode	Data Taking Mode											
		Select	0											
		Masked Channels	Untrimmable, Stuck, Dead and Noisy Channels											
	DACs	Ipreamp	220 μ A											
		Ishaper	30 μ A											
		Threshold DAC	(scanned)											
		Calibration DAC	-											
		Delay Register	(optimised)											
		TrimRange	0											
		TrimDAC	(optimised)											
	TRIGGER	Sequence	L1A											
Frequency		Up to 100kHz, depending upon occupancy												
SCANS	LOOPS	1 – THRESHOLD	0 – 150mV in 2.5mV steps (typically to cover the range $-1.0fC$ to $+2.0fC$)											
	n Triggers	Up to 1000,000, depending upon occupancy												

Analysis

This scan yields a direct measurement of noise occupancy at 1fC. The trim information is read in from the most recent results file such that the 1fC point is accurately known: in this the module currents and its noise occupancy at the nominal operating point can be extracted from the data.

By fitting an error function to the noise occupancy curve for each chip, the noise occupancy offset is determined. The response curve is read in from the most recent results file and the information is used to fit a straight line to a plot of log occupancy vs. threshold² (fC^2) to yield a measurement of the noise.

Defective channels are categorised as follows:

Defect	Description	Condition(s)
NO_HI	A channel with high noise occupancy	Occupancy $> 5 \times 10^{-4}$

^{vi} The 100kHz trigger rate and buffer overflow control have been implemented only for users of CLOAC. A fallback test has been implemented for users with only SLOG, but the trigger rate is not controlled.

Database

The following information should be stored in the SCT database:

TSTDAQINFO: host and version information
TSTDCSINFO: monitored voltages, currents and temperatures
TSTHYBNOISE: noise occupancy at 1fC, NO offset and estimated noise (ENC)

DEFECTS:

Defect	Channel	Last Channel
NO_HI	First Channel	Last Channel

Acceptance

Use of the “PASS” field is not yet implemented for this test, hence it is always set to “YES”.

The database reporting structure should provide the possibility to set acceptance cuts on each of the following parameters:

- The extrapolated noise occupancy offset,
- The mean noise occupancy at 1fC
- RMS of the noise occupancy at 1fC
- The estimated noise at 1fC
- The number of channels with low noise occupancy
- The number of channels with high noise occupancy
- The typical and maximum values of Icc and Idd.

Sample Output from the Results File

```

#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY  : pwp
LOCATION NAME   : RAL
Run number    : 256-53
TEST_DATE     : 09/08/2001
PASSED        : YES
PROBLEM       : NO
#
%DAQ_INFO
#
#HOST
"HEPNTW124"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"18:47:33"
#
%DCS_INFO
#
#T0      T1
25.5     26.3
#VDET    IDET
350      1.220
#VCC     ICC
3.500    790
#VDD     IDD
4.000    535
#
%NO
#
#MAX     ICC     IDD
        795     710
#TYP     ICC     IDD
        795     535
#
#
#      Offset MeanOcc      RMSOcc      EstENC
#M0    0.0    0.0e+000    0.0e+000    0
#S1    0.0    0.0e+000    0.0e+000    0
#S2    0.0    0.0e+000    0.0e+000    0
#S3    0.0    0.0e+000    0.0e+000    0
#S4    32.9   1.6e-005    8.6e-006    1407
#E5    31.0   1.1e-006    1.2e-006    1291
#M8    30.6   1.3e-005    5.6e-006    1458
#S9    31.5   9.6e-006    6.4e-006    1430
#S10   31.3   1.1e-005    5.4e-006    1420
#S11   31.8   7.1e-006    3.7e-006    1412
#S12   30.5   8.7e-006    5.0e-006    1416
#E13   26.4   2.7e-006    3.5e-006    1343
#
#No defects found!
#
#No raw data!

```

Timewalk.cpp

In the ABCD3T Chip specification document, timewalk is defined as, “The maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10.0fC, with the comparator set to 1fC”. This procedure sets out to make this measurement.

Method

SETTINGS	Configuration	Master/Slave/End	M	S	S	S	S	E	M	S	S	S	S	E	
		Edge Detect													ON
		Data Compression													01X
		Mode													Data Taking Mode
		Select													0
		Masked Channels													Untrimmable, Stuck, Dead and Noisy Channels
	DACs	Ipreamp													220µA
		Ishaper													30µA
		Threshold DAC													(1fC)
		Calibration DAC													(variable)
		Delay Register													(scanned)
		TrimRange													0
		TrimDAC													(optimised)
	TRIGGER	Sequence													Calibration Pulse + 131 BCO delay + L1A
Frequency														-	
SCANS	LOOPS	1 – Qinj													1.25fC, 10.0fC
		2 – Delay													0 to 63, step size = 1
	n Triggers													1000	

Analysis

For each value of injected charge, a complementary error function is fitted to the falling edge of a plot of efficiency vs. the setting of the delay register, to determine the delay setting at which the efficiency reaches half of its peak value. The difference between these two values gives the timewalk in terms of steps on the delay register.

In the case of the delay scan taken with 10fC injected charge, an error function is fitted to the rising edge of the efficiency plot. Since these scans are taken in edge mode the width of the strobe delay peak will be 25nS. This provides a calibration factor for the strobe delay register, hence the timewalk can be converted to units of nS.

Anomalous timewalk values are categorised as defects as follows:

Defect	Condition	Default value of cut
TW_LO	Timewalk < MIN_TW	5
TW_HI	Timewalk > MAX_TW	16

Database

The following information should be stored in the SCT database:

<u>TSTDAQINFO:</u>	host and version information
<u>TSTDCSINFO:</u>	monitored voltages, currents and temperatures
<u>TSTSCANINFO:</u>	number of scans and corresponding charge values
<u>TSTHYBTW:</u>	timewalk (nS) and calibration factor of each chip

DEFECTS:

Defect	First Channel	Last Channel
TW_LO	First Channel	Last Channel
TW_HI	First Channel	Last Channel

Acceptance

The "PASS" field will be set to "NO" if any defects are found.

The database reporting structure should provide the possibility to set more stringent acceptance cuts on the calculated value of the timewalk and the strobe delay calibration factor.

Sample Output from the Results File

```
#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY : pwp
LOCATION NAME : RAL
Run number : 256-55
TEST_DATE : 09/08/2001
PASSED : YES
PROBLEM : NO
#
%DAQ_INFO
#
#HOST
"HEPNTW124"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"18:58:22"
#
%DCS_INFO
#
#T0 T1
25.5 26.3
#VDET IDET
350 1.220
#VCC ICC
3.500 790
#VDD IDD
4.000 535
#
%SCAN_INFO
#
#POINT TYPE
"QCAL (fC)"
#N_POINTS
10
#POINTS
1.25 1.50 1.75 2.00 3.00 4.00 5.00 6.00
8.00 10.00
#
%Timewalk
#
#TW
#M0 S1 S2 S3 S4 E5
0.0 0.0 0.0 0.0 11.9 11.4
#
#M8 S9 S10 S11 S12 E13
11.4 11.6 11.9 11.7 11.4 10.7
#
#TCAL
#M0 S1 S2 S3 S4 E5
-1.0 -1.0 -1.0 -1.0 28.9 29.5
#
#M8 S9 S10 S11 S12 E13
28.9 28.5 29.6 28.2 29.4 30.7
#
```

```
%Defect
DEFECT NAME      : TW_LO
FIRST CHANNEL    : 0
LAST CHANNEL     : 127
#
%Defect
DEFECT NAME      : TW_LO
FIRST CHANNEL    : 128
LAST CHANNEL     : 255
#
%Defect
DEFECT NAME      : TW_LO
FIRST CHANNEL    : 256
LAST CHANNEL     : 383
#
%Defect
DEFECT NAME      : TW_LO
FIRST CHANNEL    : 384
LAST CHANNEL     : 511
#
#4 defects found
#
#No raw data!
```

Description of Other Electrical Tests

Hybrid Long Term Test

Method

For a number of hours, a hybrid is maintained such that its thermistors report a constant temperature in the region of 37°C. Periodically a characterisation test is executed, and the list of defects is compared to those which are already known. Any newly found defects are logged in the database.

Analysis

The results of each confirmation sequence will be compared against earlier data to identify the occurrence of any new defects.

Database

[TSTDAQINFO:](#) host and version information
[TSTDCSINFO:](#) monitored voltages, currents and temperatures at the end of test
[TSTHYBLTT:](#) minimum and maximum temperatures and currents during the test

DEFECTS: any defect type appropriate to confirmation sequence, but only newly occurring ones are recorded

RAW DATA:

ABCD_CONFIG (optional)
LTT_MONITOR_DATA (mandatory)

Sample Output from the Results File

```
#
%NEW_TEST
#
SERIAL NUMBER : 20220170100016
TEST MADE BY  : dgc
LOCATION NAME   : Birmingham
Run number    : 123-1
TEST_DATE     : 09/08/2001
PASSED        : YES
PROBLEM       : NO
#
%DAQ_INFO
#
#HOST
"NOTHEPNTW124"
#VERSION
"3.10"
#DUT
"Barrel Module"
#TIME
"10:00:00"
#
%DCS_INFO
#
#T0      T1
37.5     38.3
#VDET    IDET
0         0.000
#VCC     ICC
3.500    790
#VDD     IDD
4.000    535
#
%LongTermTest
#
#Duration
99.9
#Time of first failure
2.0
#T0 min max
36.4     37.5
#T1 min max
36.8     38.3
#Icc min max
780      800
#Idd min max
530      540
#
%Defect
DEFECT NAME : DEAD
FIRST CHANNEL : 128
LAST CHANNEL : 255
URL          : 10.59.23 09/08/2001
#
#1 new defect found
#
%TEST Rawdata
FILENAME    : D:\sctvar\results\20220170100016_ltt_246-1.txt
```

Appendices

Appendix 1 – Definitions of Utility Tables

TSTDAQINFO: tag "%DAQ_INFO"

Column Name		Representation	Range	Comment
HOST	O	Char(30)	-	Hostname of test PC
VERSION	O	Char(10)	-	Software Version, e.g. 3.10
DUT	O	Char(20)	-	Device Under Test eg. "Barrel Hybrid" or "Barrel Module"
TEST_TIME	O	Char(10)	-	Time the test started

TSTDCSINFO: tag "%DCS_INFO"

Column Name		Representation	Range	Comment
T0	O	Float	-100 to 200	Module Temp. 0 (°C)
T1	O	Float	-100 to 200	Module Temp. 1 (°C)
Vdet	O	Float	0 to 500	Detector Voltage (V)
Idet	O	Float	0 to 5200	Detector Current (µA)
Vcc	O	Float	0 to 10	Analogue Voltage (V)
Icc	O	Float	0 to 10	Analogue Current (A)
Vdd	O	Float	0 to 10	Digital Voltage (V)
Idd	O	Float	0 to 10	Digital Current (A)
TIME_POWERED	O	Float	0 - inf.	(hours)

TSTSCANINFO: tag "%SCAN_INFO"

Column Name		Representation	Range	Comment
POINT_TYPE	M	Char(20)	-	Scan point descriptor
N_POINTS	M	Int (8 bit)	0 to 16	Number of scans
POINT_0	O	Float	-inf to inf	Scan point setting
POINT_1	O	Float	-inf to inf	Scan point setting
POINT_2	O	Float	-inf to inf	Scan point setting
POINT_3	O	Float	-inf to inf	Scan point setting
POINT_4	O	Float	-inf to inf	Scan point setting
POINT_5	O	Float	-inf to inf	Scan point setting
POINT_6	O	Float	-inf to inf	Scan point setting
POINT_7	O	Float	-inf to inf	Scan point setting
POINT_8	O	Float	-inf to inf	Scan point setting
POINT_9	O	Float	-inf to inf	Scan point setting
POINT_10	O	Float	-inf to inf	Scan point setting
POINT_11	O	Float	-inf to inf	Scan point setting
POINT_12	O	Float	-inf to inf	Scan point setting
POINT_13	O	Float	-inf to inf	Scan point setting
POINT_14	O	Float	-inf to inf	Scan point setting
POINT_15	O	Float	-inf to inf	Scan point setting

Appendix 2 – Definitions of Result Tables

TSTMODIV: tag "%ModIVScan"

Column Name		Representation	Range	Comment
TEMPERATURE	M	Float		For compatibility with existing IV table (=T0)
I_LEAK_150	M	Float	0 to 5200	Leakage Current (μ A)
I_LEAK_350	M	Float	0 to 5200	Leakage Current (μ A)

TSTHYBRESET: tag "%HardReset"

Column Name		Representation	Range	Comment
ICC_NOCONFIG	M	Float	0 to 2000	Analogue Current (mA)
IDD_NOCONFIG	M	Float	0 to 2000	Digital Current (mA)
ICC_NOCLOCK	M	Float	0 to 2000	Analogue Current (mA)
IDD_NOCLOCK	M	Float	0 to 2000	Digital Current (mA)

TSTHYBPIPE: tag "%PipelineTest"

Column Name		Representation	Range	Comment
M0_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S1_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S2_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S3_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S4_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
E5_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
M8_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S9_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S10_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S11_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
S12_NGOOD	M	Int (8 bit)	0 to 128	No. good channels
E13_NGOOD	M	Int (8 bit)	0 to 128	No. good channels

TSTHYBBPASS: tag "%FullBypassTest"

Column Name		Representation	Range	Comment
M0_TOKEN	M	Float	0 to 10 V	
M0_RTOKEN	M	Float	0 to 10 V	
S1_TOKEN	M	Float	0 to 10 V	
S1_RTOKEN	M	Float	0 to 10 V	
S2_TOKEN	M	Float	0 to 10 V	
S2_RTOKEN	M	Float	0 to 10 V	
S3_TOKEN	M	Float	0 to 10 V	
S3_RTOKEN	M	Float	0 to 10 V	
S4_TOKEN	M	Float	0 to 10 V	
S4_RTOKEN	M	Float	0 to 10 V	FORWARD ONLY
E5_TOKEN	M	Float	0 to 10 V	FORWARD ONLY
E5_RTOKEN	M	Float	0 to 10 V	
M8_TOKEN	M	Float	0 to 10 V	
M8_RTOKEN	M	Float	0 to 10 V	
S9_TOKEN	M	Float	0 to 10 V	
S9_RTOKEN	M	Float	0 to 10 V	
S10_TOKEN	M	Float	0 to 10 V	
S10_RTOKEN	M	Float	0 to 10 V	
S11_TOKEN	M	Float	0 to 10 V	
S11_RTOKEN	M	Float	0 to 10 V	
S12_TOKEN	M	Float	0 to 10 V	
S12_RTOKEN	M	Float	0 to 10 V	FORWARD ONLY
E13_TOKEN	M	Float	0 to 10 V	FORWARD ONLY
E13_RTOKEN	M	Float	0 to 10 V	
M0_COMMENT	M	Char(20)		
M0_RCOMMENT	M	Char(20)		
S1_COMMENT	M	Char(20)		
S1_RCOMMENT	M	Char(20)		
S2_COMMENT	M	Char(20)		
S2_RCOMMENT	M	Char(20)		
S3_COMMENT	M	Char(20)		
S3_RCOMMENT	M	Char(20)		
S4_COMMENT	M	Char(20)		
S4_RCOMMENT	M	Char(20)		FORWARD ONLY
E5_COMMENT	M	Char(20)		FORWARD ONLY
E5_RCOMMENT	M	Char(20)		
M8_COMMENT	M	Char(20)		
M8_RCOMMENT	M	Char(20)		
S9_COMMENT	M	Char(20)		
S9_RCOMMENT	M	Char(20)		
S10_COMMENT	M	Char(20)		
S10_RCOMMENT	M	Char(20)		
S11_COMMENT	M	Char(20)		
S11_RCOMMENT	M	Char(20)		
S12_COMMENT	M	Char(20)		
S12_RCOMMENT	M	Char(20)		FORWARD ONLY
E13_COMMENT	M	Char(20)		FORWARD ONLY
E13_RCOMMENT	M	Char(20)		

TSTHYBDELAY: tag "%StrobeDelay"

Column Name		Representation		Comment
M0_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S1_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S2_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S3_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S4_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
E5_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
M8_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S9_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S10_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S11_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
S12_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay
E13_DELAY	M	Int (8 bit)	-1 to 63	Optimum Strobe Delay

TSTHYBRC: tags "%ThreePointGain" and "%ResponseCurve"

Column Name		Representation	Range	Comment
Loop A				
A_RC_FIT	M	Float ^{vii}	0 to 255	Fit function type
A_RC_P0	M	Float	-inf to inf	Fit parameter 0
A_RC_P1	M	Float	-inf to inf	Fit parameter 1
A_RC_P2	M	Float	-inf to inf	Fit parameter 2
Where A = {M0, S1, S2, S3, S4, E5, M8, S9, S10, S11, S12, E13}				
Loop B				
B_RC_MN_VT50	M	Float	0 to 640	Mean VT50 at 1fC (mV)
B_RC_RMS_VT50	M	Float	0 to 30	RMS VT50 at 1fC (mV)
B_RC_MN_GAIN	M	Float	0 to 100	Mean gain at 2fC (mV/fC)
B_RC_RMS_GAIN	M	Float	0 to 30	RMS gain at 2fC (mV/fC)
B_RC_MN_OFFSET	M	Float	-100 to 120	Extrapolated Offset (mV)
B_RC_RMS_OFFSET	M	Float	0 to 30	RMS Ext. Offset (mV)
B_RC_MN_NSE	M	Float	0 to 120	Mean output noise at 2fC (mV)
B_RC_MN_ENC	M	Float	0 to 5000	Mean input noise at 2fC (ENC)
B_RC_RMS_ENC	M	Float	0 to 1000	RMS input noise at 2fC (ENC)
Where B = {M0, S1, S2, S3, S4, E5, M8, S9, S10, S11, S12, E13}				
Loop C				
B_RC_COMMENT	M	Char(20)	-	Comment
Where C = {M0, S1, S2, S3, S4, E5, M8, S9, S10, S11, S12, E13}				

^{vii} For reasons of convenience when reading the table into the database

TSTHYBNOISE: tag "%NO"

Column Name		Representation	Range	Comment
ICC_MAX	M	Float	0 to 2000	Highest Icc (mA)
IDD_MAX	M	Float	0 to 2000	Highest Idd (mA)
ICC_TYP	M	Float	0 to 2000	Icc at 1fC (mA)
IDD_TYP	M	Float	0 to 2000	Idd at 1fC (mA)
Loop A				
A_NO_OFFSET	M	Float	-100 to 120	Noise occupancy offset (mV)
A_NO_MN_OCC	M	Float	0 to 1	Mean Noise occupancy at 1fC
A_NO_RMS_OCC	M	Float	0 to 1	RMS Noise occupancy at 1fC
A_NO_NSE	M	Float	0 to 5000	Estimated noise (ENC)
Where A = {M0, S1, S2, S3, S4, E5, M8, S9, S10, S11, S12, E13}				

TSTHYBTRIM: tag "%Trim"

Column Name		Representation	Range	Comment
TR_TYPE	M	Int (8 bit)	-1 to 127	Trim Type (Range)
TR_ALGORITHM	M	Int (8 bit)	0 to 255	Trim Algorithm
Loop A				
A_TR_RANGE	M	Float ^{viii}	0 to 3	Trim Range Setting
A_TR_TARGET	M	Float	0 to 640	Trim Target
A_TR_NTRIM	M	Float ^{viii}	0 to 128	Number of trimmable channels
A_TR_MN_VT50	M	Float	0 to 640	Mean VT50 after trimming (mV)
A_TR_RMS_VT50	M	Float	0 to 120	RMS VT50 After trimming (mV)
A_TR_MN_STEP	M	Float	0 to 20	Mean TrimDAC step (mV)
A_TR_RMS_STEP	M	Float	0 to 10	RMS TrimDAC step (mV)
A_TR_MNOFFSET	M	Float	-120 to 120	Mean TrimDAC Offset (mV)
A_TR_RMSOFFSET	M	Float	0 to 10	RMS TrimDAC offset (mV)
Where A = {M0, S1, S2, S3, S4, E5, M8, S9, S10, S11, S12, E13}				

^{viii} For reasons of convenience when reading the table into the database

TSTHYBTW: tag "%Timewalk"

Column Name		Representation	Range	Comment
M0_TW	M	Float	0 to 25	Timewalk (nS)
S1_TW	M	Float	0 to 25	Timewalk (nS)
S2_TW	M	Float	0 to 25	Timewalk (nS)
S3_TW	M	Float	0 to 25	Timewalk (nS)
S4_TW	M	Float	0 to 25	Timewalk (nS)
E5_TW	M	Float	0 to 25	Timewalk (nS)
M8_TW	M	Float	0 to 25	Timewalk (nS)
S9_TW	M	Float	0 to 25	Timewalk (nS)
S10_TW	M	Float	0 to 25	Timewalk (nS)
S11_TW	M	Float	0 to 25	Timewalk (nS)
S12_TW	M	Float	0 to 25	Timewalk (nS)
E13_TW	M	Float	0 to 25	Timewalk (nS)
M0_TCAL	M	Float	-1 to 63	Calibration factor
S1_TCAL	M	Float	-1 to 63	Calibration factor
S2_TCAL	M	Float	-1 to 63	Calibration factor
S3_TCAL	M	Float	-1 to 63	Calibration factor
S4_TCAL	M	Float	-1 to 63	Calibration factor
E5_TCAL	M	Float	-1 to 63	Calibration factor
M8_TCAL	M	Float	-1 to 63	Calibration factor
S9_TCAL	M	Float	-1 to 63	Calibration factor
S10_TCAL	M	Float	-1 to 63	Calibration factor
S11_TCAL	M	Float	-1 to 63	Calibration factor
S12_TCAL	M	Float	-1 to 63	Calibration factor
E13_TCAL	M	Float	-1 to 63	Calibration factor

TSTHYBLTT: tag "%LongTermTest"

Column Name		Representation	Range	Comment
Duration	M	Float	0 to 1000	Duration of test (hours)
Fail_time	M	Float	-1 to 1000	Time of first failure
T0_min	M	Float	-100 to 200	Minimum hybrid temp.
T0_max	M	Float	-100 to 200	Maximum hybrid temp.
T1_min	M	Float	-100 to 200	Minimum hybrid temp.
T1_max	M	Float	-100 to 200	Maximum hybrid temp.
Icc_min	M	Float	0 to 2000	Minimum analogue current
Icc_max	M	Float	0 to 2000	Maximum analogue current
Idd_min	M	Float	0 to 2000	Minimum digital current
Idd_max	M	Float	0 to 2000	Maximum digital current

Appendix 3 – List of Defect Names

Defect	Associated Test(s)	Associated Table(s)	First Channel	Last Channel
IV_LIMIT	IVCurve.cpp	TSTMODIV	0	1535
IV_TRIP			0	1535
HR_NOCLK	HardReset.cpp	TSTHYBRESET	Link * 768	((Link+1)*768)-1
HR_NOCON			Link * 768	((Link+1)*768)-1
HR_NORST			Link * 768	((Link+1)*768)-1
CLK_ADDR0	RedundancyTest.cpp	TSTHYBCLOCK	Chip * 128	((Chip+1)*128)-1
CLK_ADDR1			Chip * 128	((Chip+1)*128)-1
CLK_COM0			Chip * 128	((Chip+1)*128)-1
CLK_COM1			Chip * 128	((Chip+1)*128)-1
CLK_ERROR			Chip * 128	((Chip+1)*128)-1
TOKEN	FullBypassTest.cpp	TSTHYBBPASS	Chip * 128	((Chip+1)*128)-1
RTOKEN			Chip * 128	((Chip+1)*128)-1
DEAD	PipelineTest.cpp	TSTHYBPIPE	Channel	Channel
STUCK			Channel	Channel
DEADCELL			Channel	Channel
STUCKCELL			Channel	Channel
SD_LO	StrobeDelay.cpp	TSTHYBDELAY	Chip * 128	((Chip+1)*128)-1
SD_HI			Chip * 128	((Chip+1)*128)-1
DEAD	ThreePointGain.cpp ResponseCurve.cpp	TSTHYBRC	First Channel	Last Channel
STUCK			First Channel	Last Channel
LO_GAIN			First Channel	Last Channel
HI_GAIN			First Channel	Last Channel
LO_OFFSET			First Channel	Last Channel
HI_OFFSET			First Channel	Last Channel
UNBONDED			First Channel	Last Channel
PARTBONDED			First Channel	Last Channel
NOISY			First Channel	Last Channel
INEFF			First Channel	Last Channel
TR_RANGE			TrimRange.cpp	TSTHYBTRIM
TR_STEP	First Channel	Last Channel		
TR_OFFSET	First Channel	Last Channel		
NO_HI	NO.cpp	TSTHYBNOISE	First Channel	Last Channel
TW_LO	Timewalk.cpp	TSTHYBTW	First Channel	Last Channel
TW_HI			First Channel	Last Channel

Appendix 4 – Database table implementation status

Table	Table approved for addition to DB	Priority	Table added to the DB	File format approved for Java Application	Java Application Implemented
TSTDAQINFO	NOT YET	-	-	-	-
TSTDCSINFO	NOT YET	-	-	-	-
TSTSCANINFO	NOT YET	-	-	-	-
TSTMODIV	<i>Already exists as TSTDETIV</i>				
TSTHYBRESET	NOT YET	-	-	-	-
TSTHYBCLOCK	NOT YET	-	-	-	-
TSTHYBBPASS	NOT YET	-	-	-	-
TSTHYBPIPE	NOT YET	-	-	-	-
TSTHYBDELAY	NOT YET	-	-	-	-
TSTHYBRC	NOT YET	-	-	-	-
TSTHYBTRIM	NOT YET	-	-	-	-
TSTHYBNOISE	NOT YET	-	-	-	-
TSTHYBTW	NOT YET	-	-	-	-
TSTHYBLTT	NOT YET	-	-	-	-

References

¹ <http://sct-testdaq.home.cern.ch/sct-testdaq/sctdaq/sctdaq.html>